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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/927,457	08/13/2001	Laurent Fournier	FOURNIER=1	4159

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BROWDY AND NEIMARK, P.L.L.C.
624 NINTH STREET, NW
SUITE 300
WASHINGTON, DC 20001-5303

EXAMINER

KENDALL, CHUCK O

ART UNIT	PAPER NUMBER
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2122

DATE MAILED: 08/26/2004

6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/927,457

Applicant(s)

FOURNIER, LAURENT

Examiner

Chuck Kendall

Art Unit

2122

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 August 2001.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-35 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed 10/09/01.
2. Claims 1 – 35 have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 - 35 rejected under 35 U.S.C. 102(b) as being anticipated by Bujanos USPN 5,570,664.

Regarding claim 1, Bujanos anticipates, an apparatus for implementing a Floating-Point related application, comprising:

a tool that includes: a receiver for receiving a list of commands in a computer language (4:1 – 3, see receive program instructions and transfer data);

the language defining Floating-Point events of interest in respect of at least one FP instruction (9: 27 – 42, see “C”-language and double character);

a parser for parsing the commands (9: 20 – 25, see traverse);

a processor configured to process at least the parsed commands for realizing the floating-point related application on the basis of said events (9:20 – 30).

Regarding claim 2, the apparatus of claim 1, wherein said language further defining regrouping of the events into at least one coverage model; and

wherein said processor is configured to process the parsed commands for realizing the floating-point related application on the basis of said events and said at least one coverage model (9:20 – 30).

Regarding claim 3, the apparatus according to claim 1, wherein said application is an evaluation of coverage of tests being run on a design (11:25 – 35).

Regarding claim 4, the apparatus according to claim 1, wherein said processor is configured to generate a sequence of test vectors for verification of Floating-Point module operation (11: 5 –15, see check tests test vectors);

the test vectors meet the constraints of said events (2:32 – 36, see condition for constraints).

Regarding claim 5, the apparatus according to claim 4, wherein said verification includes verifying if the Floating-Point operation complies with IEEE standard for Floating-Point (2:27 –32).

Regarding claim 6, for use with the Floating-Point module of claim 1, a computer language;

the language defining Floating-Point events of interest in respect of at least one FP instruction (11:10 –15, for language see verilog).

Regarding claim 7, the computer language of claim 6, further defining regrouping of the events into at least one coverage model (7:48 –65, see classify and grouping of instructions).

Regarding claim 8, an apparatus for implementing a Floating-Point related application, comprising:

a tool that includes:

a receiver for receiving a list of commands in a computer language (4:1 – 3, see receive program instructions and transfer data);

the language defining Floating-Point events of interest and regrouping of events into at least one coverage model, in respect of at least one FP instruction (9: 27 – 42, see “C”- language and double character);

the coverage model having the form of a sequence of Floating-Point commands with constraints on (i) at least one intermediate result operand of the FP instruction, and (ii) result operand of the FP instruction(9:20 – 30);

a parser for parsing the commands(9: 20 – 25, see traverse);

a processor for processing at least the parsed commands for realizing the Floating-point related application at least on the basis of said events and said at least one coverage model(9:20 – 30).

Regarding claim 9, which sites similarly to claim 2, see reasoning as previously discussed above.

Regarding claim 10, which sites similarly to claim 3, see reasoning as previously discussed above.

Regarding claim 11, which sites similarly to 5, see reasoning as previously discussed above.

Regarding claim 12, for use with the Floating-Point module of claim 8, a computer language;

the language defining Floating-Point events of interest and regrouping of events into at least one coverage model, in respect of at least one FP instruction, the coverage model having the form of a sequence of Floating-Point commands with constraints on (i) at least one intermediate result operand of the FP instruction, and (ii) result operand of the FP instruction (9: 27 – 55, see "C"-language and double character); .

Regarding claim 13, which sites similarly to claim 1, see reasoning as previously discussed above.

Regarding claim 14, which sites similarly to claim 3, see reasoning as previously discussed above.

Regarding claim 15, which sites similarly to claim 4, see reasoning as previously discussed above.

Regarding claim 16, which sites similarly to claim 5, see reasoning as previously discussed above.

Regarding claim 17, which sites similarly to claim 12, see reasoning as previously discussed above.

Regarding claim 18, the apparatus according to claim 1, wherein said list of commands includes:

range of FP numbers (10:35 – 60);

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mask on bits of FP number (FIG. 9, 272, and associated text);
set or Reset Number of Bits in an FP number (FIG. 9, 274, and associated text);
set or Reset Continuous-Bit-Long in an FP number (FIG. 9, 270, and associated text);

relative Values of at least two FP numbers, and logical operations among said Commands (10: 60 – 65).

Regarding claim 19, which sites similarly to claim 18 see reasoning as previously discussed above.

Regarding claim 20, which sites similarly to claim 18 see reasoning as previously discussed above.

Regarding claim 21, which sites similarly to claim 18 see reasoning as previously discussed above.

Regarding claim 22, which sites similarly to claim 18 see reasoning as previously discussed above.

Regarding claim 23, which sites similarly to claim 18, see reasoning as previously discussed above.

Regarding claim 24, which sites similarly to claim 18 above, see reasoning as previously discussed above.

Regarding claim 25, the apparatus according to claim 8, wherein said constraints are further applied to attributes of Machine State (10: 1 – 10, for Machine state, see execution of requested FPU instruction using an assembly level instruction).

Regarding claim 26, the apparatus according to claim 25, wherein said constraints are further applied to attributes of Machine State (10: 1 – 10, for Machine state, see execution of requested FPU instruction using an assembly level instruction).

Regarding claim 27, which is the method version of claim 1, see reasoning as previously discussed above.

Regarding claim 28, which is the method version of claim 8, see reasoning as previously discussed above.

Regarding claim 29, which sites similarly to claim 8, see reasoning as previously discussed above.

Regarding claim 30, which is the storage device version of claim 1, see reasoning as previously discussed above.

Regarding claim 31, which is the program product version of claim 1, see reasoning as previously discussed above.

Regarding claim 32, which is the storage device version of claim 8, see reasoning as previously discussed above.

Regarding claim 33, which is the program product version of claim 8, see reasoning as previously discussed above.

Regarding claim 34, which is the machine readable version of claim 8, see reasoning as previously discussed above.

Regarding claim 35, which also cites similarly as claim 33 is the program product version of claim 8, see reasoning above as previously discussed.

Correspondence Information

5. Any inquires concerning this communication or earlier communications from the examiner should be directed to Chuck O. Kendall who may be reached via telephone at (703) 308-6608. The examiner can normally be reached Monday through Friday between 8:00 A.M. and 5:00 P.M. est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam *can be* reached at (703) 305-4552.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

For facsimile (fax) send to 703-7467239 official and 703-7467240
draft
CK.



**ANTHONY NGUYEN-BA
PRIMARY EXAMINER**